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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/783,779	02/14/2001	Srinivas Chennupaty	42390P10924	3051
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN			KIM, KENNETH S	
12400 WILSHI LOS ANGELES	RE BOULEVARD, SEVI S. CA 90025	ENTH FLOOR	OR ART UNIT PAPER NUMBER	
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DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-	Арри	cation No.	Applicant(s)			
		33,779	CHENNUPATY ET AL.			
Office Action Summary		iner	Art Unit			
		eth S KIM	2111			
The MAILING DATE of this co Period for Reply	mmunication appears o	n the cover sheet with the	correspondence address			
A SHORTENED STATUTORY PER THE MAILING DATE OF THIS COM  - Extensions of time may be available under the professor of time of the mailing date of the second of the period for reply specified above is less than a lift NO period for reply is specified above, the max failure to reply within the set or extended period any reply received by the Office later than three earned patent term adjustment. See 37 CFR 1.7	IMUNICATION. rovisions of 37 CFR 1.136(a). In a ris communication. It hirty (30) days, a reply within the imum statutory period will apply a for reply will, by statute, cause the months after the mailing date of the control of the cause the cause the months after the mailing date of the cause th	no event, however, may a reply be ting statutory minimum of thirty (30) day and will expire SIX (6) MONTHS from a BANDONE application to become ABANDONE	mely filed ys will be considered timely. n the mailing date of this communication. ED (35 U.S.C. § 133).			
Status						
1) Responsive to communication	(s) filed on <u>24 May 200</u>	<u>4</u> .				
2a) This action is <b>FINAL</b> .	2b)⊠ This action					
3) Since this application is in con	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the	practice under <i>Ex parte</i>	e <i>Quayle</i> , 1935 C.D. 11, 4	53 O.G. 213.			
Disposition of Claims						
4)	_ is/are withdrawn from <u>41</u> is/are rejected. I to.	consideration.	KENNETH S. KIM			
Application Papers						
9) The specification is objected to 10) The drawing(s) filed oni Applicant may not request that an Replacement drawing sheet(s) inc 11) The oath or declaration is object	s/are: a) ☐ accepted o y objection to the drawing cluding the correction is re	(s) be held in abeyance. Se quired if the drawing(s) is ob	e 37 CFR 1.85(a). ojected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a a) All b) Some * c) None 1. Certified copies of the p 2. Certified copies of the p 3. Copies of the certified copies of the period copies of the certified copies of the pieces.	e of: riority documents have riority documents have opies of the priority documents have rnational Bureau (PCT	been received. been received in Applicati uments have been receive Rule 17.2(a)).	ion No ed in this National Stage			
Attachment(s)  1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Re 3) Information Disclosure Statement(s) (PTO-1 Paper No(s)/Mail Date		4) Interview Summary Paper No(s)/Mail Do 5) Notice of Informal F 6) Other:				
U.S. Palent and Trademark Office PTOL-326 (Rev. 1-04)	Office Action Sun		art of Paper No./Mail Date 070920(			

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- 1. Claims 1-16, 23-25, and 31-41 remain are for examination.
- 2. Claims 1-16, 23-25, 31-33, and 35-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Hansen, U.S. Patent No. 5,819,117, cited in the previous office action.

<u>Hansen</u> teaches the invention as claimed in claim 1 including a computer system (figs. 3B and 10C) comprising:

- (a) a processor (50),
- (b) a storage device coupled to the processor (40) and having stored therein an instruction, when executed by the processor, causes the processor to at least,
- (c) access a packed data operand (fig. 10C, 71) having at least two portion of data elements (bytes 0-3 and 4-7),
- (d) select a set of data elements from a portion of the packed data operand, the portion including at least two data elements (b(0) to b(3)),
- (e) copy each data element of the selected set of data elements to specified data fields located in the corresponding portion of the destination operand (74), and

further teaches as in claims 2-5,

- (f) wherein the packed data operand includes eight data elements (b(0) to b(7)) and the processor selects a set of data elements from either the upper half or the lower half (b(0) to b(3)) claim 2,
- (g) wherein a packing device packs integer data to the data elements of 16-bits (can be any bit size) to 128 bit operand claims 3 and 4, and

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(h) the data packed and destination operands are the same operand (destination can be the source operand) – claim 5.

The method claims 6-10, the image data processing method claims 11-16 (with well known three dimensional transformation data processing), and the program product claims 23-25, the method claims 31 and 32, the processor claims 33 and 35 for three instructions, the method claims 36-38, and the processor claims 39 and 40 are equivalently rejected based on the same reason.

3. Claims 1-16, 23-25, and 31-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Sidwell, U.S. Patent No. 5,822,619, cited in the previous office action.

Sidwell teaches the invention as claimed in claim 1 including a computer system (figs. 1 and 7) comprising:

- (a) a processor (fig. 1),
- (b) a storage device coupled to the processor (10) and having stored therein an instruction, when executed by the processor, causes the processor to at least,
- (c) access a packed data operand (fig. 7; data format 4n2v1p) having at least two portion of data elements (bytes 0-3 and 4-7),
- (d) select a set of data elements from a portion of the packed data operand, the portion including at least two data elements (bytes 0-3 or 4-7; col. 8, line 42)
- (e) copy each data element of the selected set of data elements to specified data fields located in the corresponding portion of the destination operand (fig. 9, 132), and further teaches as in claims 2-5,

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(f) wherein the packed data operand includes eight data elements (bytes 0-7) and the processor selects a set of data elements from either the upper half or the lower half (bytes 0-3 or 4-7; col. 8, line 42) – claim 2,

- (g) wherein a packing device packs integer data to the data elements of 16-bits (can be any bit size) to 128 bit operand claims 3 and 4, and
- (h) the data packed and destination operands are the same operand (destination can be the source operand) claim 5.

The method claims 6-10, the image data processing method claims 11-16 (with well known three dimensional transformation data processing), and the program product claims 23-25, the method claims 31 and 32, the processor claims 33-35 for three instructions with upper and lower half operations (col. 8, line 42), the method claims 36-38, and the processor claims 39-41 with upper and lower half operations are equivalently rejected based on the same reason.

- The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claims 1-16, 23-25, and 31-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abdallah et al, U.S. Patent No. 6,192,476 in view of Huff et al, U.S. patent No. 6,288,723, both cited in the previous office action.

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Abdallah et al teaches the invention substantially as claimed in claim 1 including a computer system (figs. 2A) comprising:

- (a) a processor (fig. 205),
- (b) a storage device coupled to the processor (285) and having stored therein an instruction, when executed by the processor, causes the processor to at least,
- (c) access a packed data operand (col. 3, line 20) having at least two portion of data elements (subsets, col. 3, line 19),
- (d) select a set of data elements from a portion of the packed data operand, the portion including at least two data elements (subset, col. 3, line 19), and

further teaches as in claims 2-5,

- (f) wherein the packed data operand includes eight data elements (can be any number; col. 10, lines 53-56) and the processor selects a set of data elements from either the upper half or the lower half (upper and lower subset) claim 2,
- (g) wherein a packing device packs integer data to the data elements of 16-bits (can be any bit size) to 128 bit operand claims 3 and 4, and
- (h) the data packed and destination operands are the same operand (col. 7, line 54) claim 5,

however, does not expressly state that each data element of the selected set of data elements are copied to specified data fields located in the corresponding portion of the destination operand, while teaching ADD and MUL operations on the selected set of data elements (i.e., partial width operations).

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Huff et al teaches the method of copying each data element of the selected set of data elements to specified data fields located in a destination operand (fig. 3E),

It would have been obvious to a person of ordinary skill in the art at the time the invention was made that the partial width operation can be any type of operation (Abdallah et al; col. 10, line 16) including the copying operation. The person would have been motivated to provide a partial width copying operation for enhanced versatility.

The method claims 6-10, the image data processing method claims 11-16 (with well known three dimensional transformation data processing), and the program product claims 23-25, the method claims 31 and 32, the processor claims 33-35 for three instructions for upper and lower portion operations (col. 13, line 25), the method claims 36-38, and the processor claims 39-41 with upper and lower portion operations (are equivalently rejected based on the same reason.

6. Applicant's argument filed May 24, 2004 has been considered but they are not persuasive.

Applicant argued that the load operation in <u>Hansen</u> is between a 32-bit source memory operand and 64 bit register operand and thus the 32-bit does not constitute a *portion* of a source operand and that the source and the destination operand cannot be the same.

The reference indicates that the 32-bit constitutes the lower order bytes or the higher order bytes (col. 14, lines 58 and 62) and thus showing the copying of data from a portion of memory operand to a corresponding portion of register operand.

The reference teaches the selective copying operation of data elements while loading and the selective copying operation can be done from a source operand to a destination operand which are the same. The method of using a source operand as the destination operand is well known in the art (see Abdallah et al, col. 7, line 54).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth S KIM whose telephone number is (703) 305-9693. The examiner can normally be reached on M-F (8:30-17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

July 9, 2004

KENNETH S. MIN

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